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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,449	06/18/2001	Nai-Yin Sung	TS00-415	2688

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,449	SUNG ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/17/2004 has been entered.

Claims 1-6, 8-18 and 20 are pending.

Claim Rejections - 35 USC § 103

1. Claims 1-4, 6, 8-11, 13-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, and in view of Takahashi Ohsawa, U.S. Patent No. 5748641.

As per Claims 1, 8 and 13:

The emulation method and apparatus taught in Lu specifies a system which introduces known fault data into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST..." (Abstract and column 5 lines 1-21). Lu teaches in the Abstract and column 6 lines 45-48 an "apparatus for verifying the effectiveness of a RAM BIST..." by "...introducing known fault data into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST...". In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2)

address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 6 lines 45-46 teaches that there is "...comparing the results of said RAM system model with said known fault data.". But the memory unit model lacks a de-scrambler. In the analogous art of Ohsawa, a scrambler and a de-scrambler are put to use in a memory test configuration, where data and address are scrambled and de-scrambled at the inputs and outputs of the memory device (see Ohsawa Abstract). The reference also states in column 2 lines 19-47 the advantage of the invention as solving the drawbacks of testing DRAMs containing address and data sensitive patterns by scrambling and de-scrambling the same during test. One with ordinary skill in the art at the time of the invention, motivated as suggested by Ohsawa, would find it to be obvious to combine the two references in order to achieve the advantage stated, and so the claims are rejected.

As per claims 2 and 9:

Lu teaches in column 3 lines 45-48 that the fault file comprises of a "...record for each of the addresses...". According to the Microsoft Computer Dictionary, 3rd edition, 1997, a "database" file is defined as "A file composed of records..." Therefore, Lu teaches that the fault file is a database file, as is claimed by the applicant, and in view of the motivation previously stated, the claims are rejected.

As per claims 3 and 10:

Lu teaches in column 2 lines 59-63 of his specification, "Modeling RAM behavior...can be performed by any type of modeling tool. However, a hardware modeling language such as VHDL currently provides the most efficient means of carrying out the invention." Therefore, Lu teaches the use of VHDL in the memory behavior model, and in view of the motivation previously stated, the claims are rejected.

As per claims 4 and 11:

Lu teaches in his column 5 lines 21-25 that the mask values (set of faults) in the fault database "...indicating bit faults..." in the form of "stuck" 1's or 0's. Therefore, Lu teaches all of the points in the applicant's claims, and in view of the motivation previously stated, the claims are rejected..

As per Claims 6 and 18:

Lu substantially teaches a method/apparatus for verifying the effectiveness of a RAM BIST in Claims 1 and 13. What Lu does not specifically teach is the scrambling and descrambling of address and data to and from the memory behavior model. Ohsawa (see column 9 lines 45-67 and column 10 lines 1-3), in describing the scrambling and de-scrambling patent, teaches that the testing of DRAM memories may include these functions in order to more completely test and verify memory (column 2 lines 19-47). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu to include scrambling and descrambling in order to incorporate full memory testing to the extent that is taught by Oshawa. One would have been motivated as recited by Ohshawa in

Claim 1 in order to scramble and unscramble memories such as are claimed, and so the claims are rejected.

As per claim 14:

Lu teaches in column 3 lines 45-48 that the fault file comprises of a "...record for each of the addresses...". According to the Microsoft Computer Dictionary, 3rd edition, 1997, a "database" file is defined as "A file composed of records...". Therefore, Lu teaches that the fault file is a database file, as is also claimed by the applicant. In view of the previously stated motivation, the claim is rejected.

As per claim 15:

Lu teaches in column 2 lines 59-63 of his specification, "Modeling RAM behavior...can be performed by any type of modeling tool. However, a hardware modeling language such as VHDL currently provides the most efficient means of carrying out the invention." Therefore, Lu teaches the use of VHDL in the memory behavior model, and in view of the previous motivation, the claim is rejected.

As per claim 16:

Lu teaches in column 6 lines 47-51 that the mask values (set of faults) in the fault database "...indicating bit faults..." in the form of "stuck" 1's or 0's. Therefore, Lu teaches all of the points in the applicant's claim 16, and in view of previous motivation, the claim is rejected.

2. Claims 5, 12, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, and in view of Takahashi Ohsawa,

U.S. Patent No. 5748641 as applied to Claims 1, 8 and 13 above, and further in view SynTest Technologies, Inc., March 1999.

As per Claims 5, 12 and 17:

Lu teaches in his specification in column 4, lines 4 to 9 the execution by the BIST controller of a diagnostic program named "14N March". Lu fails to describe this diagnostic as "March C+" as the applicant specifies in the application. But, this diagnostic, 14N March, is defined and referred to also as "March C+" by SynTest Technologies (see "SynTest Enters the BIST Product", SynTest Technolgies, Inc., March 1999, http://www.syntest.com/PressReleaseArchive/19990308_2.htm). And in the 2nd paragraph of that publication, the advantage is recited to be reducing the time and effort required to design, test and develop embedded RAMs. Therefore, one with ordinary skill in the art at the time of the invention, motivated by SynTest as suggested, would apply the use of the diagnostic "March C+" in the specification above by Lu, and so the claims are rejected.

As per Claim 20:

Lu teaches all of the aspects of the applicant's Claim 13, but Lu however fails to specify the makeup of the BIST circuit model, which is specified by the applicant's claim 20 as being an RTL or gate level design. SynTest Technologies is a memory BIST Technology Company, and it conducts the business of modeling BIST's for clients. In their press release of March 1999, their BIST model was specified as being an "RTL product". Therefore, it would have been obvious to a person in the art at the time of the invention, that RTL modeling of BIST circuits is common in the marketplace. And

motivated by SynTest as stated previously, it would have been the natural choice of one versed in the art at that time to include an RTL model in the design of a BIST controller in order offer to the public an "industry standard" design, and so the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

ALBERT DECADY
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